REMARKS

Applicant respectfully requests further examination and reconsideration in view of the arguments set forth fully below. Claims 1-46 were previously pending in this application. Within the Office Action, Claims 1-46 have been rejected. By the above amendment, Claims 1, 9, 17, 25, 33, and 40 have been amended. Claims 1-46 are now pending in the application.

Rejections Under 35 U.S.C. § 102

Within the Office Action, Claims 1-46 excluding Claims 5, 8, 13, 16, 21, 24, 29, 32, 36, 39, 43, and 46 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,515,329 to Dalton et al. (hereinafter "Dalton"). The Applicant respectfully disagrees with this rejection.

Dalton teaches a memory system 10 including an input FIFO 12, an output FIFO 13, a DSP 11, and a DRAM array 15. The input FIFO 12 buffers input to the DSP 11 and the output FIFO 13 buffers output from the DSP 11. The DRAM array 15 is coupled to the DSP 11 to provide additional buffering capability (Dalton, col. 1, lines 31-32). The memory system 10 operates in two modes, a non-buffering mode and a buffering mode. In the non-buffering mode, data is sent from the input FIFO 12 to the output FIFO 13 without involving the DRAM array 15 (Dalton, bottom of page including columns 3 and 4). Interrupts are triggered when particular capacity conditions are reached within either the input FIFO 12, the output FIFO 13, or both. Triggering of the interrupts initiates data transfer from either the input FIFO 12 to the DRAM array 15, or from the DRAM array 15 to the output FIFO 13 depending on the particular interrupt triggered. The DSP 11 provides all DRAM control. The DSP 11 also performs operations on the data "between the input FIFO and the output FIFO" (Dalton, col. 1, lines 28-29). Dalton does not teach performing operations on the data while the data is **within** a FIFO buffer.

Further, Dalton clearly differentiates between a FIFO memory and a DRAM array. In column 2, lines 6-7, Dalton states that "..the DSP is in the process of providing FIFO and DRAM services." As such, the memory system 10 of Dalton requires both FIFO memory and DRAM arrays, which are admittedly distinguishable from each other. In contrast, the present invention is directed exclusively to a FIFO memory.

In contrast to the teachings of Dalton, the programmable first-in first-out buffer of the present invention receives a stream of data to be buffered within the first-in first-out buffer, while the stream of data is still within the first-in first-out buffer. The programmable first-in first-out

buffer includes the ability to receive program instructions from an application or control circuit to perform specific operations on the stream of data before the data is provided as an output from the programmable first-in first-out buffer. By performing the specific operations of the program instructions on the stored data while the stored data is within the first-in first-out buffer, the programmable first-in first-out buffer has the ability to filter the stream of data as it passes through the first-in first-out buffer, including re-ordering data within the first-in first-out buffer, if appropriate, and also to synchronize the input and output of the stream of data with external input and output signals, respectively. As discussed above, Dalton does not teach performing operations on the data while the data is **within** a first-in first-out buffer. Further, Dalton is directed to both first-in first-out memory and DRAM arrays. Each of the independent Claims 1, 9, 17, 25, 33, and 40 have been amended to clarify that the stream of data stored in the first-in first-out buffer is manipulated while the stored stream of data is within the first-in first-out buffer.

The independent Claim 1 is directed to a method of buffering data within a first-in first-out buffer. The method of Claim 1 comprises receiving a stream of data to be buffered within the first-in first-out buffer, storing the stream of data within the first-in first-out buffer thereby forming a stored stream of data, obtaining a series of program instructions at the first-in first-out buffer specifying operations to be performed on the stored stream of data, and generating an output stream of data by executing the series of program instructions and performing the operations to manipulate the stored stream of data while within the first-in first-out buffer. As discussed above, Dalton does not teach performing operations on the data while the data is within a first-in first-out buffer. Further, Dalton is directed to both first-in first-out memory and DRAM arrays. For at least these reasons, the independent Claim 1 is allowable over the teachings of Dalton.

Claims 2-4, 6, and 7 are dependent on the independent Claim 1. As described above, the independent Claim 1 is allowable over the teachings of Dalton. Accordingly, Claims 2-4, 6, and 7 are all also allowable as being dependent on an allowable claim.

The independent Claim 9 is directed to a method of buffering data within a first-in first-out buffer. The method of Claim 9 comprises receiving a stream of data to be buffered within the first-in first-out buffer, storing the stream of data within the first-in first-out buffer thereby forming a stored stream of data, obtaining a series of program instructions at the first-in first-out buffer specifying operations to be performed in relation to the stored stream of data and generating an output stream of data by executing the series of program instructions and performing the operations to manipulate the stored stream of data while within the first-in first-

out buffer, including synchronizing the output stream of data to a time reference. As discussed above, Dalton does not teach performing operations on the data while the data is within a first-in first-out buffer. Further, Dalton is directed to both first-in first-out memory and DRAM arrays. For at least these reasons, the independent Claim 9 is allowable over the teachings of Dalton.

Claims 10-12, 14 and 15 are dependent on the independent Claim 9. As described above, the independent Claim 9 is allowable over the teachings of Dalton. Accordingly, Claims 10-12, 14 and 15 are all also allowable as being dependent on an allowable claim.

The independent Claim 17 is directed to an apparatus for buffering data within a first-in first-out buffer. The apparatus of Claim 17 comprises means for receiving a stream of data to be buffered within the first-in first-out buffer, means for storing the stream of data within the first-in first-out buffer thereby forming a stored stream of data, means for obtaining a series of program instructions specifying operations to be performed on the stored stream of data and means for generating an output stream of data by executing the series of program instructions and performing the operations to manipulate the stored stream of data while within the first-in first-out buffer. As discussed above, Dalton does not teach performing operations on the data while the data is within a first-in first-out buffer. Further, Dalton is directed to both first-in first-out memory and DRAM arrays. For at least these reasons, the independent Claim 17 is allowable over the teachings of Dalton.

Claims 18-20, 22, and 23 are dependent on the independent Claim 17. As described above, the independent Claim 17 is allowable over the teachings of Dalton. Accordingly, Claims 18-20, 22, and 23 are all also allowable as being dependent on an allowable claim.

The independent Claim 25 is directed to a programmable first-in first-out buffer. The programmable first-in first-out buffer of Claim 25 comprises an input interface circuit configured to receive a stream of data to be buffered within the first-in first-out buffer, a data memory coupled to the input interface circuit to store the stream of data, thereby forming a stored stream of data, a program memory configured to obtain and store a series of program instructions specifying operations to be performed on the stored stream of data and an execution unit coupled to the program memory and to the data memory to generate an output stream of data by executing the series of program instructions and perform the operations on the stored stream of data while the stored stream of data is within the data memory of the first-in first-out buffer. As discussed above, Dalton does not teach performing operations on the data while the data is within a first-in first-out buffer. Further, Dalton is directed to both first-in first-out memory and DRAM arrays. For at least these reasons, the independent Claim 25 is allowable over the teachings of Dalton.

Claims 26-28, 30, and 31 are dependent on the independent Claim 25. As described above, the independent Claim 25 is allowable over the teachings of Dalton. Accordingly, Claims 26-28, 30, and 31 are all also allowable as being dependent on an allowable claim.

The independent Claim 33 is directed to a system comprising a bus interface circuit configured to couple to a bus structure and receive a stream of data, a data memory coupled to the bus interface circuit to store the stream of data, thereby forming a stored stream of data, wherein the data memory stores and outputs the stored stream of data, thereby forming an output stream of data, a program memory configured to obtain and store a series of program instructions specifying operations to be performed on the stored stream of data and an execution unit coupled to the program memory and to the data memory to generate the output stream of data by executing the series of program instructions and performing the operations on the stored stream of data while the stored stream of data is within the data memory. As discussed above, Dalton does not teach performing operations on the data while the data is within a first-in first-out buffer. Further, Dalton is directed to both first-in first-out memory and DRAM arrays. For at least these reasons, the independent Claim 33 is allowable over the teachings of Dalton.

Claims 34, 35, 37, and 38 are dependent on the independent Claim 33. As described above, the independent Claim 33 is allowable over the teachings of Dalton. Accordingly, Claims 34, 35, 37, and 38 are all also allowable as being dependent on an allowable claim.

The independent Claim 40 is directed to a network of devices. The network of devices of Claim 40 comprises a plurality of devices, a bus structure coupled between the plurality of devices to transmit data between the devices and a programmable first-in first-out buffer including an input interface circuit configured to receive a stream of data to be buffered within the first-in first-out buffer, a data memory coupled to the input interface circuit to store the stream of data, thereby forming a stored stream of data, a program memory configured to obtain and store a series of program instructions specifying operations to be performed on the stored stream of data and an execution unit coupled to the program memory and to the data memory to generate the output stream of data by executing the series of program instructions and perform the operations on the stored stream of data while the stored stream of data is within the data memory of the first-in first-out buffer. As discussed above, Dalton does not teach performing operations on the data while the data is within a first-in first-out buffer. Further, Dalton is directed to both first-in first-out memory and DRAM arrays. For at least these reasons, the independent Claim 40 is allowable over the teachings of Dalton.

Claims 41, 42, 44, and 45 are dependent on the independent Claim 40. As described above, the independent Claim 40 is allowable over the teachings of Dalton. Accordingly, Claims 41, 42, 44, and 45 are all also allowable as being dependent on an allowable claim.

Within the Office Action, Claims 1-46 excluding Claims 5, 8, 13, 16, 21, 24, 29, 32, 36, 39, 43, and 46 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,732,223 to Johnson. The Applicant respectfully disagrees with this rejection. The Applicant points out that Johnson does not appear to be a proper 102(b) reference.

Johnson teaches a memory access system including a plurality of FIFO buffers 12, a write counter 4 and a write address decoder 8 to write data to the FIFO buffers 12, and a read counter 6 and a read address decoder 10 to read data from the FIFO buffers 12. Data is written into the FIFO buffers 12 according to address write pointers determined by the write counter 4 and the write address decoder 8. Data is read from the FIFO buffers 12 according to address read pointers determined by the read counter 6 and the read address decoder 10. The read pointers and the write pointers are manipulated to reference sequential buffers within the FIFO buffers 12 in order to cause a minimum of one buffer position offset between the read and write pointers (Johnson, col. 5, line 62 to col. 6, line 33). In summary, Johnson teaches manipulating the read and write pointers referencing FIFO buffers (Johnson, col. 6, lines 34-51). Johnson does not teach manipulating the data stored within the FIFO buffers. Further, Johnson does not teach manipulating the data stored in the FIFO buffers while the data is still within the FIFO buffers. As discussed above, each of the independent Claims 1, 9, 17, 25, 33, and 40 have been amended to clarify that the stream of data stored in the first-in first-out buffer is manipulated while the stored stream of data is within the first-in first-out buffer.

The independent Claim 1 is directed to a method of buffering data within a first-in first-out buffer. The method of Claim 1 comprises receiving a stream of data to be buffered within the first-in first-out buffer, storing the stream of data within the first-in first-out buffer thereby forming a stored stream of data, obtaining a series of program instructions at the first-in first-out buffer specifying operations to be performed on the stored stream of data, and generating an output stream of data by executing the series of program instructions and performing the operations to manipulate the stored stream of data while within the first-in first-out buffer. As discussed above, Johnson does not teach manipulating the data stored within the FIFO buffers. Further, Johnson does not teach manipulating the data stored in the FIFO buffers while the data is still within the FIFO buffers. For at least these reasons, the independent Claim 1 is allowable over the teachings of Johnson.

Claims 2-4, 6, and 7 are dependent on the independent Claim 1. As described above, the independent Claim 1 is allowable over the teachings of Johnson. Accordingly, Claims 2-4, 6, and 7 are all also allowable as being dependent on an allowable claim.

The independent Claim 9 is directed to a method of buffering data within a first-in first-out buffer. The method of Claim 9 comprises receiving a stream of data to be buffered within the first-in first-out buffer, storing the stream of data within the first-in first-out buffer thereby forming a stored stream of data, obtaining a series of program instructions at the first-in first-out buffer specifying operations to be performed in relation to the stored stream of data and generating an output stream of data by executing the series of program instructions and performing the operations to manipulate the stored stream of data while within the first-in first-out buffer, including synchronizing the output stream of data to a time reference. As discussed above, Johnson does not teach manipulating the data stored within the FIFO buffers. Further, Johnson does not teach manipulating the data stored in the FIFO buffers while the data is still within the FIFO buffers. For at least these reasons, the independent Claim 9 is allowable over the teachings of Johnson.

Claims 10-12, 14 and 15 are dependent on the independent Claim 9. As described above, the independent Claim 9 is allowable over the teachings of Johnson. Accordingly, Claims 10-12, 14 and 15 are all also allowable as being dependent on an allowable claim.

The independent Claim 17 is directed to an apparatus for buffering data within a first-in first-out buffer. The apparatus of Claim 17 comprises means for receiving a stream of data to be buffered within the first-in first-out buffer, means for storing the stream of data within the first-in first-out buffer thereby forming a stored stream of data, means for obtaining a series of program instructions specifying operations to be performed on the stored stream of data and means for generating an output stream of data by executing the series of program instructions and performing the operations to manipulate the stored stream of data while within the first-in first-out buffer. As discussed above, Johnson does not teach manipulating the data stored within the FIFO buffers. Further, Johnson does not teach manipulating the data stored in the FIFO buffers while the data is still within the FIFO buffers. For at least these reasons, the independent Claim 17 is allowable over the teachings of Johnson.

Claims 18-20, 22, and 23 are dependent on the independent Claim 17. As described above, the independent Claim 17 is allowable over the teachings of Johnson. Accordingly, Claims 18-20, 22, and 23 are all also allowable as being dependent on an allowable claim.

The independent Claim 25 is directed to a programmable first-in first-out buffer. The programmable first-in first-out buffer of Claim 25 comprises an input interface circuit configured

to receive a stream of data to be buffered within the first-in first-out buffer, a data memory coupled to the input interface circuit to store the stream of data, thereby forming a stored stream of data, a program memory configured to obtain and store a series of program instructions specifying operations to be performed on the stored stream of data and an execution unit coupled to the program memory and to the data memory to generate an output stream of data by executing the series of program instructions and perform the operations on the stored stream of data while the stored stream of data is within the data memory of the first-in first-out buffer. As discussed above, Johnson does not teach manipulating the data stored within the FIFO buffers. Further, Johnson does not teach manipulating the data stored in the FIFO buffers while the data is still within the FIFO buffers. For at least these reasons, the independent Claim 25 is allowable over the teachings of Johnson.

Claims 26-28, 30, and 31 are dependent on the independent Claim 25. As described above, the independent Claim 25 is allowable over the teachings of Johnson. Accordingly, Claims 26-28, 30, and 31 are all also allowable as being dependent on an allowable claim.

The independent Claim 33 is directed to a system comprising a bus interface circuit configured to couple to a bus structure and receive a stream of data, a data memory coupled to the bus interface circuit to store the stream of data, thereby forming a stored stream of data, wherein the data memory stores and outputs the stored stream of data, thereby forming an output stream of data, a program memory configured to obtain and store a series of program instructions specifying operations to be performed on the stored stream of data and an execution unit coupled to the program memory and to the data memory to generate the output stream of data by executing the series of program instructions and performing the operations on the stored stream of data while the stored stream of data is within the data memory. As discussed above, Johnson does not teach manipulating the data stored within the FIFO buffers. Further, Johnson does not teach manipulating the data stored in the FIFO buffers while the data is still within the FIFO buffers. For at least these reasons, the independent Claim 33 is allowable over the teachings of Johnson.

Claims 34, 35, 37, and 38 are dependent on the independent Claim 33. As described above, the independent Claim 33 is allowable over the teachings of Johnson. Accordingly, Claims 34, 35, 37, and 38 are all also allowable as being dependent on an allowable claim.

The independent Claim 40 is directed to a network of devices. The network of devices of Claim 40 comprises a plurality of devices, a bus structure coupled between the plurality of devices to transmit data between the devices and a programmable first-in first-out buffer including an input interface circuit configured to receive a stream of data to be buffered within

the first-in first-out buffer, a data memory coupled to the input interface circuit to store the stream of data, thereby forming a stored stream of data, a program memory configured to obtain and store a series of program instructions specifying operations to be performed on the stored stream of data and an execution unit coupled to the program memory and to the data memory to generate the output stream of data by executing the series of program instructions and performing the operations on the stored stream of data while the stored stream of data is within the data memory of the first-in first-out buffer. As discussed above, Johnson does not teach manipulating the data stored within the FIFO buffers. Further, Johnson does not teach manipulating the data stored in the FIFO buffers while the data is still within the FIFO buffers. For at least these reasons, the independent Claim 40 is allowable over the teachings of Johnson.

Claims 41, 42, 44, and 45 are dependent on the independent Claim 40. As described above, the independent Claim 40 is allowable over the teachings of Johnson. Accordingly, Claims 41, 42, 44, and 45 are all also allowable as being dependent on an allowable claim.

Rejections under 35 U.S.C. §103

Within the Office Action, Claims 5, 8, 13, 16, 21, 24, 29, 32, 36, 39, 43 and 46 have been rejected under 35 U.S.C. §103(a) as being obvious over Dalton or Johnson. The Applicant respectfully disagrees with this rejection.

Claims 5 and 8 are dependent upon the independent Claim 1. As discussed above, Claim 1 is allowable over the teachings of Dalton and Johnson. Accordingly, Claims 5 and 8 are both also allowable as being dependent upon an allowable base claim.

Claims 13 and 16 are dependent upon the independent Claim 9. As discussed above, Claim 9 is allowable over the teachings of Dalton and Johnson. Accordingly, Claims 13 and 16 are both also allowable as being dependent upon an allowable base claim.

Claims 21 and 24 are dependent upon the independent Claim 17. As discussed above, Claim 17 is allowable over the teachings of Dalton and Johnson. Accordingly, Claims 21 and 24 are both also allowable as being dependent upon an allowable base claim.

Claims 29 and 32 are dependent upon the independent Claim 25. As discussed above, Claim 25 is allowable over the teachings of Dalton and Johnson. Accordingly, Claims 29 and 32 are both also allowable as being dependent upon an allowable base claim.

Claims 36 and 39 are dependent upon the independent Claim 33. As discussed above, Claim 33 is allowable over the teachings of Dalton and Johnson. Accordingly, Claims 36 and 39 are both also allowable as being dependent upon an allowable base claim.

Claims 43 and 46 are dependent upon the independent Claim 40. As discussed above, Claim 40 is allowable over the teachings of Dalton and Johnson. Accordingly, Claims 43 and 46 are both also allowable as being dependent upon an allowable base claim.

For the reasons given above, the Applicant respectfully submits that Claims 1-46 are now in a condition for allowance, and allowance at an early date would be appreciated. Should the Examiner have any questions or comments, they are encouraged to call the undersigned at (408) 530-9700 to discuss the same so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,
HAVERSTOCK & OWENS LLP

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By: Jonathan O. Owens

Jonathan O. Owens
Reg. No. 37,902
Attorneys for Applicant(s)

CERTIFICATE OF MAILING (37 CFR§ 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450

HAVERSTOCK & OWENS LLP.

Dated: 11-15-04 By: Jun D. Rosen